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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,756	07/24/2003	Kevin Traynor	032674-200	1739

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
02/24/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/21/2009 Amendment*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application Status

Applicants' RCE filed 1/21/2009 to continue prosecution of this application is acknowledged.

Claim Rejections - 35 USC § 112

Claims 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 28 is directed to an apparatus. However, the essential structural cooperative relationship(s) between the "processor," "interrupt source," and "interrupt input" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function

simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

Further, in claim 28, it is unclear whether "at least one interrupt source" refers to the "K input sources" already recited in claim 24. Also, it is unclear whether "at least one interrupt input" refers to the "N inputs" already recited in claim 24.

In claim 29, the term, "the processor" does not have any antecedent basis. Claim 24 does not recite any "processor."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 24-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Wash (5,530,875).

With regard to claim 24, Wash discloses a system for sharing interrupt controller inputs, said system comprising: K input sources, wherein K is an integer value; an interrupt controller having N inputs, wherein N is an integer value less than K (Wash discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure 3, which is reproduced below for ease of reference and convenience.

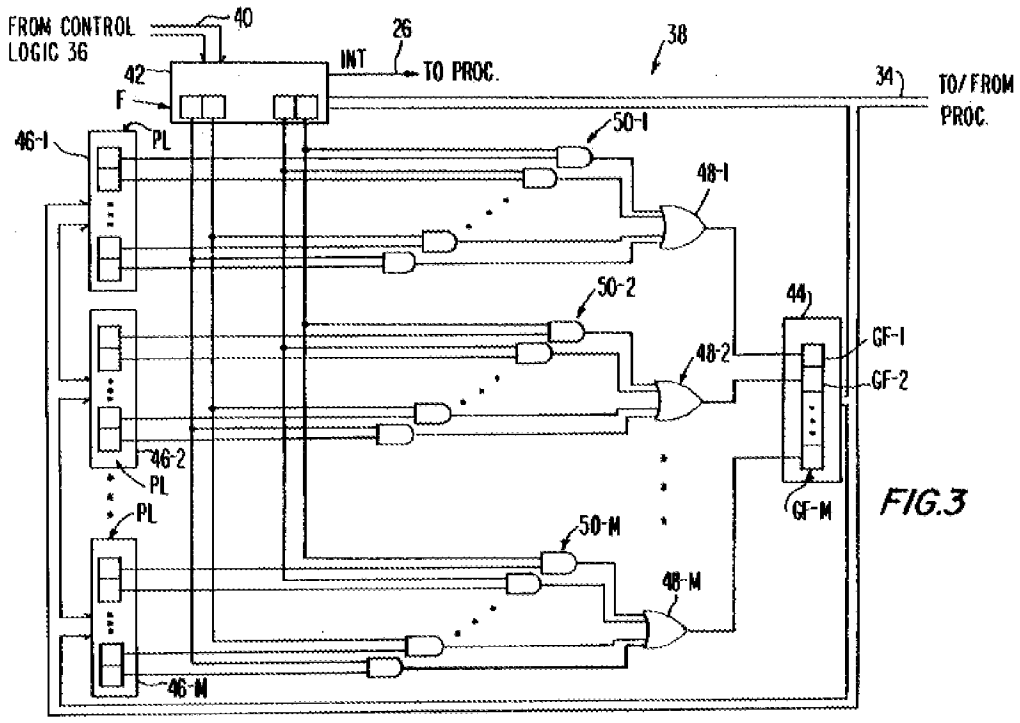

FIG.3

In Wash, the interrupt requests can be generated from either register 44 or register 42 (see column 11, lines 10-15). In addition, the term “group” used in Wash includes group that has only one interrupt resource or a plurality of interrupt sources (see discussion and citation below). As shown above and specifically described in column 2, lines 38-51, column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt sources are routed or mapped to a plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 of the

interrupt controller or interrupt manager 38; wherein the interrupt requests are selectively enabled based on the priority of the interrupt inputs. In Wash, as shown in Fig. 3 above, when the interrupt requests from interrupt sources are received at (mapped to) the interrupt inputs GF of the group register 44 of the interrupt controller or manager 38. Further, in Wash, priorities among interrupt sources are established by assigning at least one of the interrupt sources to a first priority group GF1, and assigning the remaining interrupt sources to at least a second priority group GF2. The step of assigning at least one interrupt source to a first priority group includes connecting one of the storage locations F of the interrupt register 42 with one of the storage locations GF of the group register 44. The first group represented by storage location GF1 of group register 44, the second group is represented by storage location GF2 of group register 44. See at least column 2, lines 22-28 and 41-51; column 3, lines 1-10; column 5, lines 2-40; column 6, lines 9-43; column 11, lines 47-49; column 6, lines 48-52; column 10, lines 32-50; claims 1-9.); N logical mapping subsets corresponding to the N inputs of the interrupt controller, said logical mapping subsets including: K logical ANDs having respective first inputs, second inputs and outputs, said first inputs being coupled to the K input sources, respectively, a logical OR having a plurality inputs coupled to the output of the K logical ANDs within the respective logical mapping subset, and an output coupled to the corresponding input of the interrupt controller; and N control bit sets corresponding to the N logical mapping subsets, respectively, said control bit sets having K control bits coupled to the second input of the K logical ANDs in

the corresponding logical mapping subset (Wash further discloses a plurality of the so-called “subsets” corresponding to the plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 of the interrupt controller or interrupt manager 38; wherein each of the so-called “subsets” in Wash includes a plurality of AND gates 50 each having a first input to receive an interrupt request signal from an interrupt source(s) to interrupt the processor; a second input coupled a plurality of control bits or masking bits of the so-called “control bit sets” (46 (1-M)) corresponding to the so-called "subsets", each bit can be set in the location PL to provide a control value to the second input of AND gate 50; and an output coupled to an OR gate 48; and wherein each of the so-called “subsets” also includes an OR gate 48 coupled to the plurality of outputs from the AND gates 50 of the respective subset, and an output coupled to a corresponding interrupt input of the interrupt controller 38; and based on the control bit value provided at one input of the AND gate, an interrupt request signal is provided at output of the AND gate 50. In other words, the control bit acts as a masking bit to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked).

With regard to claim 25, it is clear from Wash and discussion above that a register is used for storing the control bit values.

With regard to claim 26, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be set according to user preferences.

With regard to claim 27, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be dynamically modified according to user preferences.

With regard to claim 28, it is clear that the control bit values must be defined according to system requirements. Further, it is also clear that the system of Wash comprises the processor, at least one interrupt source, and at least one interrupt input.

With regard to claim 29, it is clear from Wash and discussion above that the processor is part of a microcontroller unit.

Response to Arguments

Applicants' arguments filed 1/21/2009 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification

cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986). With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

With regard to new claim 24, Applicants have argued that Wash does not disclose "'N control bit sets corresponding to the N logical mapping subsets, respectively, said control bit sets having K control bits coupled to the second input of the K logical ANDs in the corresponding logical mapping subset.' Wach discloses a register 42 that receives signals from control logic 36 and stores the signals in locations F. However, locations F are connected to each of the OR gates 48 that output to group flag register 44. Accordingly, locations F cannot be considered to correspond to the claimed "N control bit sets corresponding to the N logical mapping subsets, respectively," as recited in claim 24."

Contrary to Applicants' argument, it is clear that a plurality of location GF of register 44 is readable as a plurality of interrupt inputs; and that register 44 is a part of the interrupt manager 38. As disclosed in [0012], page 4 of Applicants' originally filed specification and as shown in Fig. 3, the interrupt inputs are defined as follows:

[0012] In yet another aspect of the invention, a system is disclosed for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources. The system comprises, for each interrupt input, a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor. A plurality of control bits each correspond to an interrupt source and each respectively provide a control bit value to the corresponding logical AND, wherein, based on the control bit value, a corresponding interrupt request signal is provided at an output of the corresponding logical AND. A logical OR is arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs.

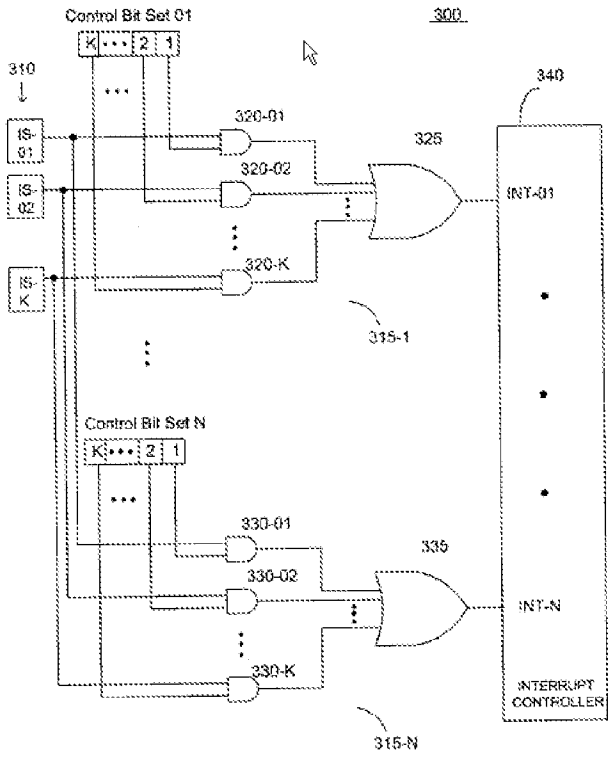

FIG. 3

Identically disclosed and shown in Fig. 3 of Wach:

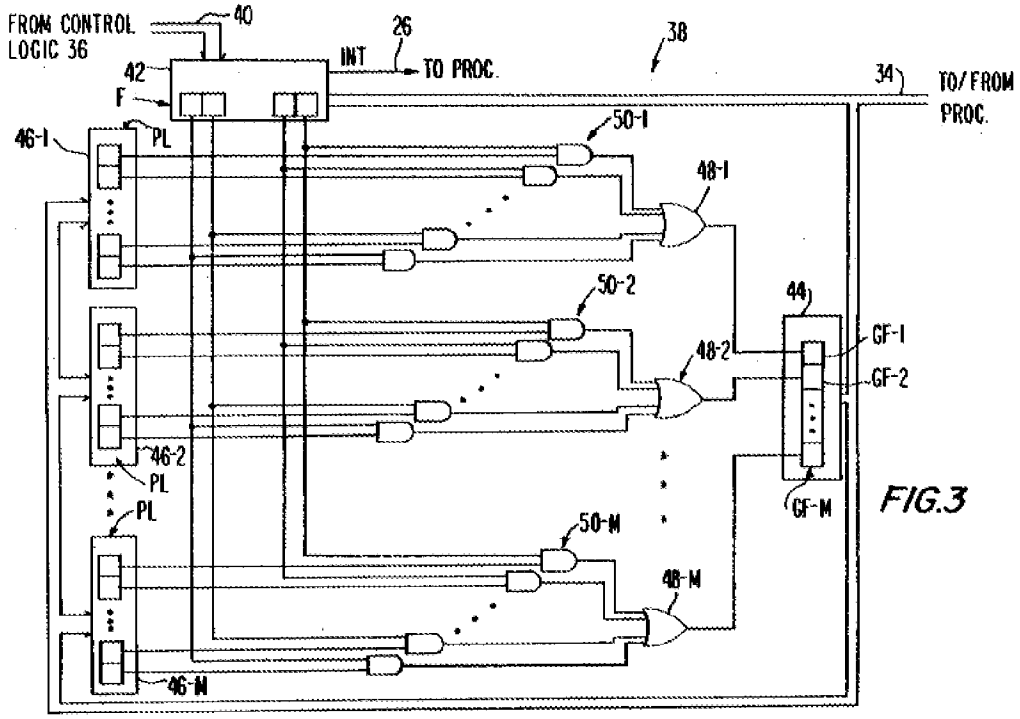

FIG.3

It is clear from at least Fig. 3 of Wach, a logical OR is arranged to indicate, to the locations GF or interrupt inputs of the interrupt controller 44 of the interrupt manager 38, the presence of a corresponding interrupt request signal from at least one output of a plurality of logical AND gates. Further, Wash further discloses a plurality of the so-called “subsets” corresponding to the plurality of interrupt inputs represented by a plurality of storage locations GF of the group register 44 of the interrupt controller or interrupt manager 38; wherein each of the so-called “subsets” in Wash includes a plurality of AND gates 50 each having a first input to receive an interrupt request signal from an interrupt source(s) to interrupt the processor; a second input coupled a plurality of control bits or masking bits of the so-called “control bit sets” (46 (1-M))

corresponding to the so-called "subsets", each bit can be set in the location PL to provide a control value to the second input of AND gate 50; and an output coupled to an OR gate 48; and wherein each of the so-called “subsets” also includes an OR gate 48 coupled to the plurality of outputs from the AND gates 50 of the respective subset, and an output coupled to a corresponding interrupt input of the interrupt controller 38; and based on the control bit value provided at one input of the AND gate, an interrupt request signal is provided at output of the AND gate 50. In other words, the control bit acts as a masking bit to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Khanh Dang/

Primary Examiner, Art Unit 2111